FIG. 1

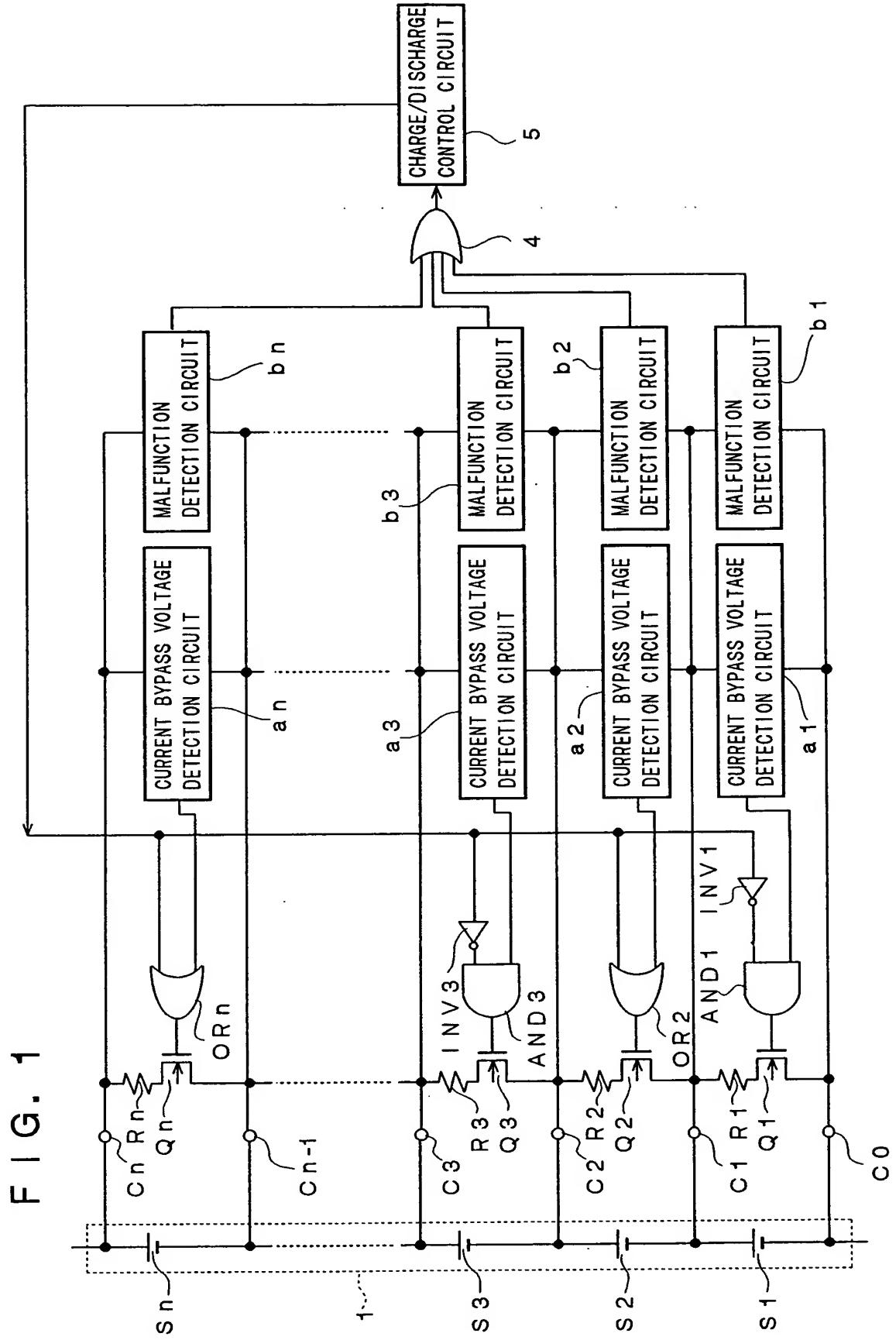

CHARGE/DISCHARGE CONTROL CIRCUIT
5
4
MALFUNCTION DETECTION CIRCUIT
CURRENT BYPASS VOLTAGE DETECTION CIRCUIT
bn
an
b3
a3
b2
a2
b1
a1
ORn
INV3
AND3
OR2
AND1
INV1
Cn
Rn
Qn
Cn-1
C3
R3
Q3
C2
R2
Q2
C1
R1
Q1
C0
Sn
1
S3
S2
S1

FIG. 2

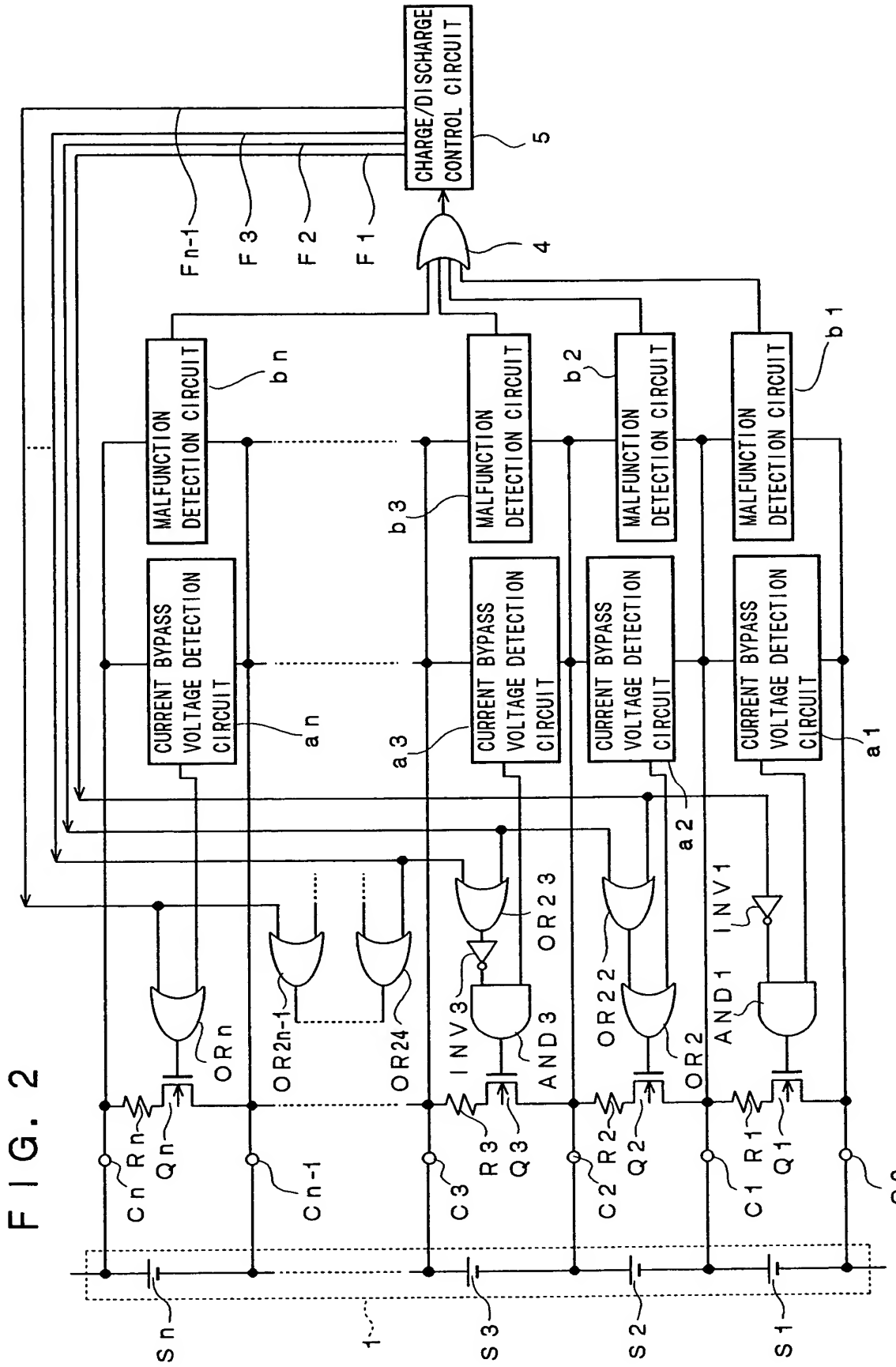

CHARGE/DISCHARGE CONTROL CIRCUIT
5
4
Fn-1
F3
F2
F1
MALFUNCTION DETECTION CIRCUIT
bn
b3
b2
b1
CURRENT BYPASS VOLTAGE DETECTION CIRCUIT
an
a3
a2
a1
ORn
OR2n-1
OR24
INV3
OR23
AND3
OR22
OR2
AND1
INV1
Cn
Rn
Qn
Cn-1
C3
R3
Q3
C2
R2
Q2
C1
R1
Q1
C0
Sn
1
S3
S2
S1

FIG. 3

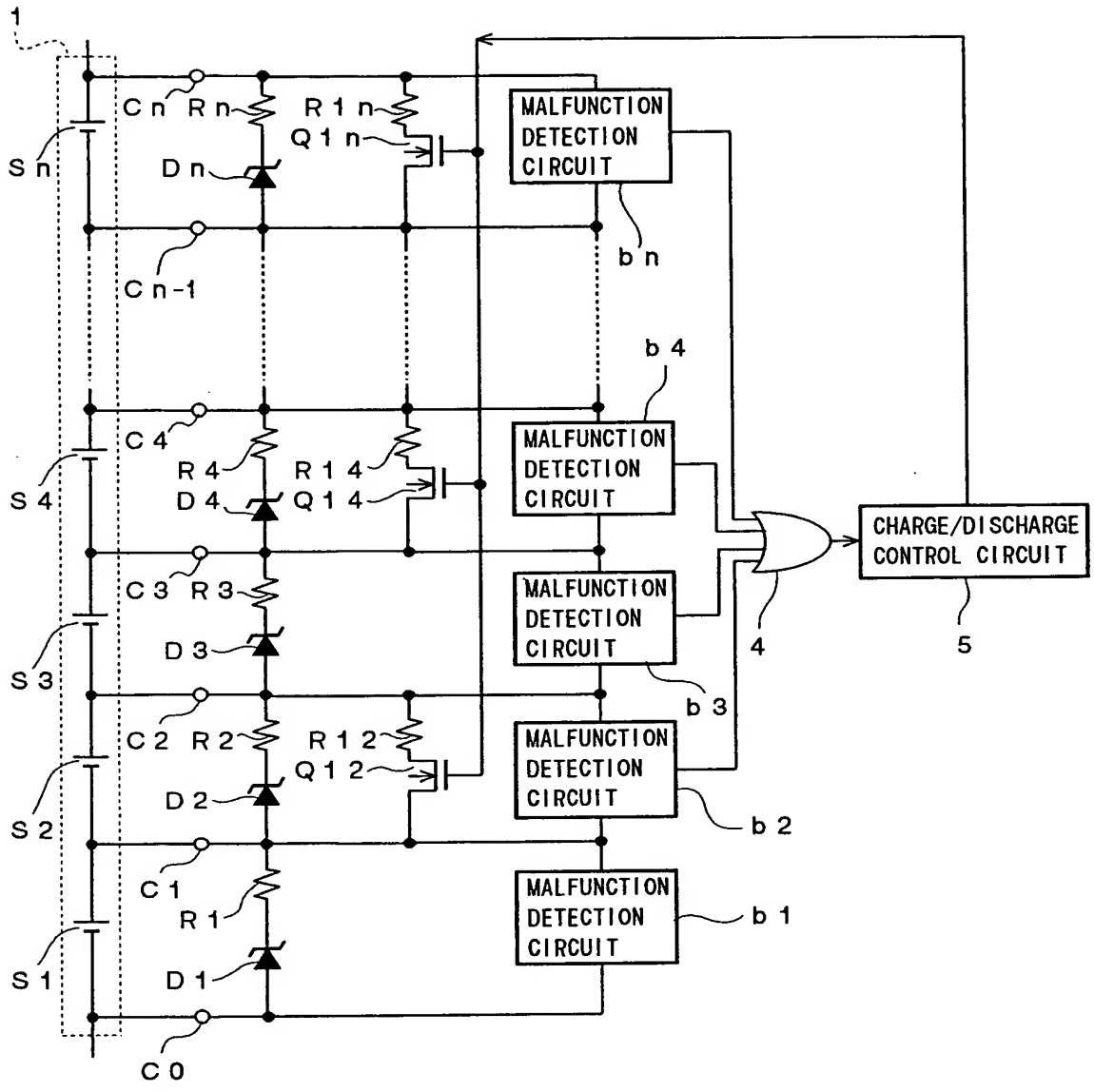

1
Cn
Rn
R1n
Q1n
Dn
Sn
Cn-1
MALFUNCTION DETECTION CIRCUIT
bn
b4
C4
R4
R14
D4
Q14
S4
C3
R3
D3
S3
C2
R2
R12
Q12
D2
S2
C1
R1
D1
S1
C0
b3
b2
b1
4
CHARGE/DISCHARGE CONTROL CIRCUIT
5

FIG. 4

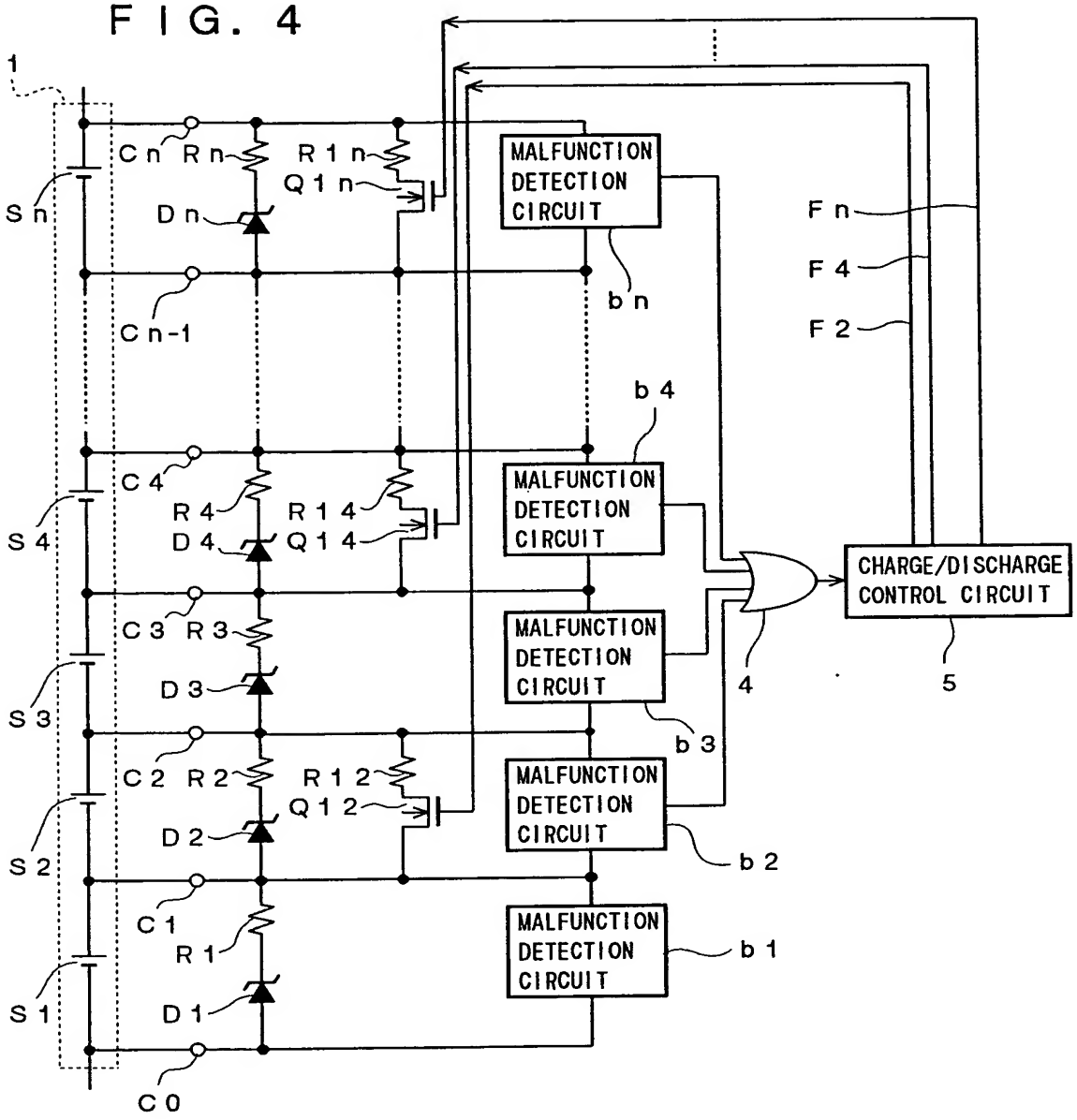

1
Cn
Rn
R1n
Q1n
Sn
Dn
MALFUNCTION DETECTION CIRCUIT
Fn
F4
F2
bn
Cn-1
b4
C4
R4
R14
Q14
S4
D4
CHARGE/DISCHARGE CONTROL CIRCUIT
C3
R3
D3
S3
4
5
b3
C2
R2
R12
Q12
D2
S2
b2
C1
R1
b1
S1
D1
C0

FIG. 5

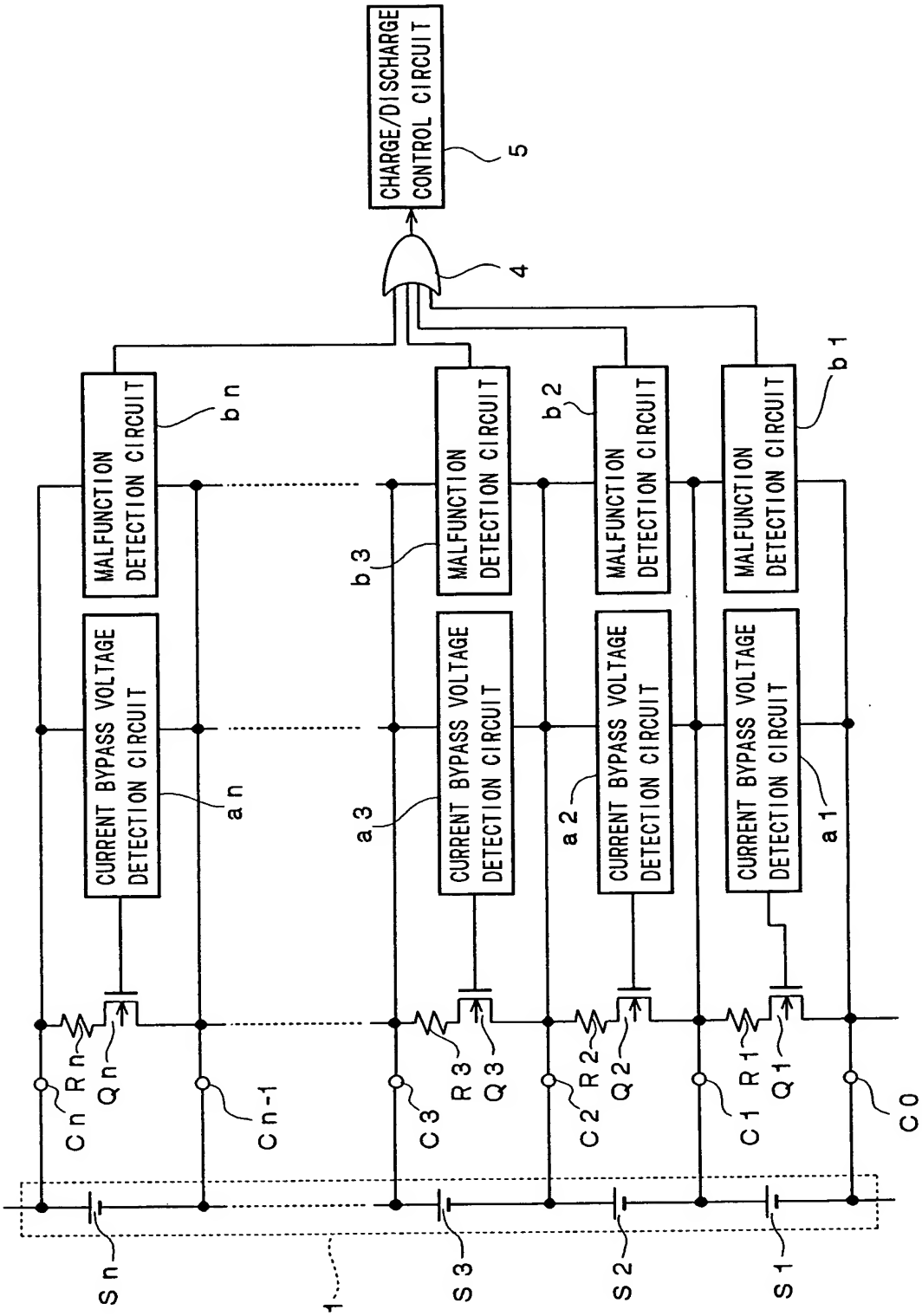
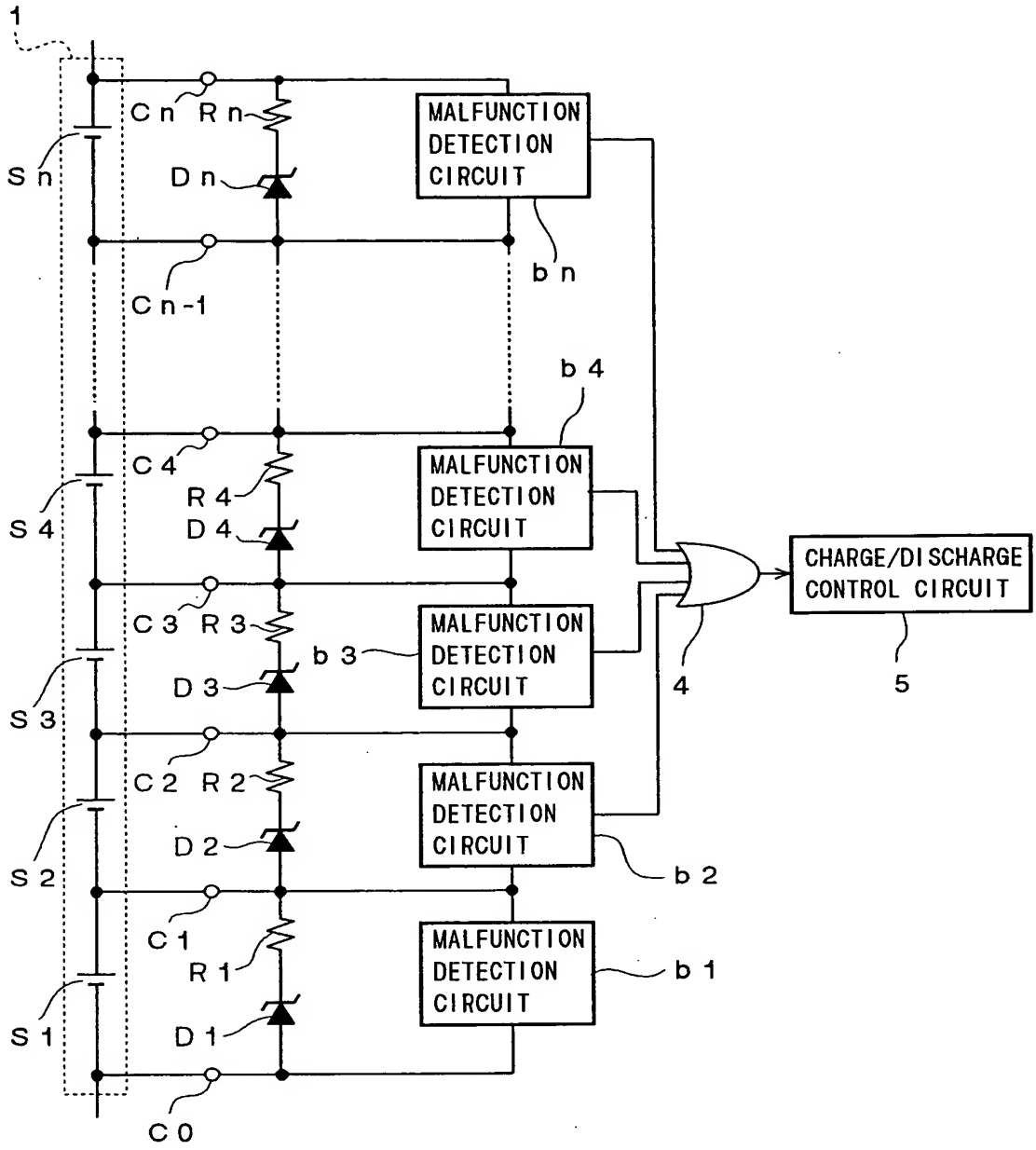

CHARGE/DISCHARGE CONTROL CIRCUIT
5
4
MALFUNCTION DETECTION CIRCUIT
CURRENT BYPASS VOLTAGE DETECTION CIRCUIT
bn
an
b3
a3
b2
a2
b1
a1
Cn
Rn
Qn
Cn-1
C3
R3
Q3
C2
R2
Q2
C1
R1
Q1
C0
Sn
S3
S2
S1
1

FIG. 6


1
Cn
Rn
Sn
Dn
MALFUNCTION DETECTION CIRCUIT
bn
Cn-1
b4
C4
R4
S4
D4
MALFUNCTION DETECTION CIRCUIT
C3
R3
b3
S3
D3
MALFUNCTION DETECTION CIRCUIT
C2
R2
S2
D2
MALFUNCTION DETECTION CIRCUIT
b2
C1
R1
S1
D1
MALFUNCTION DETECTION CIRCUIT
b1
C0
4
CHARGE/DISCHARGE CONTROL CIRCUIT
5